REMARKS

Claims 9, 11, 12 and 16-25 are pending in the present application, were examined, and stand rejected. In response, no claims are amended, no claims are cancelled and no claims are added. Applicant respectfully requests reconsideration of pending Claims 9, 11, 12 and 16-25 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Claims Rejected Under Nonstatutory Double Patenting

The Examiner has rejected Claims 9, 11-12 and 16-25 on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 1-21 of U.S. Patent 6,925,534. In response, Applicants submit a terminal disclaimer over Claims 1-21 of U.S. Patent 6,925,534 to overcome the obviousness type double patenting rejection of Claims 9, 11-12 and 16-25.

II. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claim 23 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,477,621 issued to Lee et al. ("Lee"). Applicant respectfully traverses this rejection.

Regarding Claim 23, Claim 23 recites the following claim features, which are neither disclosed, taught nor suggested by Lee:

> at least two memory modules, each memory module including:
> at least one memory device, and
> a data cache coupled to an eviction buffer, both coupled to the memory device. (Emphasis added.)

According to the Examiner:

> Lee discloses a system memory (1009, figure 5) comprising at least two memory modules (300a through 300n, figure 5), each memory modules including at least one memory device (301-304, figure 3) and a data cache (601, figure 3) coupled to the an eviction buffer (701, figure 3), both coupled to the memory device (col. 8 lines 7-42). (pg. 5, ¶5 of the Office Action mailed August 9, 2006.)

Applicant respectfully disagrees with the Examiner's contention that Lee discloses the system memory, as recited by Claim 23. To anticipate the features of Claim 23, the Examiner relies on system memory 1009, as shown in FIG. 5, as well as virtual channel system 320 of memory system 300 as shown in FIG. 3 of Lee. According to the Examiner, cache row address register 701 discloses the eviction buffer recited by Claim 23. Applicant respectfully disagrees.

Regarding the system memory 1009 disclosed by Lee with reference to FIG. 5:

> PC 1000 implements a multi-tasking system memory 1009 in accordance with the previously described embodiments. System memory 1009 includes a plurality of parallel connected memory systems 300*a*-300*n*, each of which is substantially identical to previously described memory system 300 (FIG. 3). (Col. 15, lines 8-13.) (Emphasis added.)

Lee teaches that system memory 1009 includes a plurality of parallel connected memory system 300*a*-300*n* which are substantially identical to the previously described memory system 300, as shown in FIG. 3 of Lee. Based on the cited passage above, the multi-tasking system memory 1009, as shown in FIG. 5 of Lee, is comprised of multiple memory systems 300, as shown in FIG. 3.

Consequently, the memory system 300, as shown in FIG. 3 of Lee, is not a memory module as indicated by the Examiner. Hence, Applicant respectfully submits that the plurality of parallel connected memory systems 300*a*-300*n* of multi-tasking system memory 1009, as shown in FIGS. 3 and 5 of Lee, do not disclose the at least two memory modules recited by Claim 23.

Furthermore, cache row address registers 701-707, as shown in Fig. 3 of Lee, neither disclose, teach nor suggest the eviction buffer recited by Claim 23. As disclosed by Lee:

> Each of channel row cache memories 601-607 is associated with a corresponding one of cache row address registers 701-707. Each of cache row address registers 701-707 stores N cache addresses. That is, each cache entry in channel row cache memories 601-607 has a corresponding cache address stored in a corresponding one of cache row address registers 701-707. (Col. 8, lines 41-47.)

As mandated by case law, "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik v. American Hoist & Derrick ("Lindemann"), 730 F.2d

452, 1458 (Fed. Cir. 1994) (emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. Titanium Metals Corp. of American v. Banner ("Banner Titanium"), 778 F.2d 775, 777 (Fed. Cir. 1985).

Here, the Examiner relies on the multi-tasking system memory 1009, as shown in FIG. 5 of Lee, to disclose the at least two memory modules recited by Claim 23. According to the Examiner, the plurality of parallel connected memory systems 300*a*-300*n*, as taught by Lee (see the memory system 300 shown in FIG. 3,) disclose the at least two memory modules recited by Claim 23.

Applicant respectfully submits that the memory system 300 as shown in FIG. 3, as well as the parallel connected memory systems 300*a*-300*n* as shown in FIG. 5, are clearly not memory modules, as recited by Claim 23. Apposite to the at least two memory modules recited by Claim 23, memory system 300 (FIG. 3), as well as memory systems 300*a*-300*n* (FIG. 5) are each a memory system used to form the multi-tasking system memory 1000 as shown in FIG. 5 of Lee. Accordingly, Applicant respectfully submits that the parallel connected memory system 300*a*-300*n* of multi-tasking system memory 1009 neither discloses, teaches or suggests the at least two memory modules recited by Claim 23.

Furthermore, the Examiner relies on cache row address registers 701-707 to disclose the eviction buffer recited by Claim 23. However, as explicitly disclosed by Lee, the cache row address registers 701-707 store N cache addresses. (See col. 8, lines 41-44.) As disclosed by Lee, each cache entry in channel row cache memory 601-607 has a corresponding cache address stored in a corresponding one of the cache row address registers 701-707. (See col. 8, lines 44-47.) Consequently, since Lee teaches that cache row address registers 701-707 are used to store a cache address corresponding to each cache entry within channel row cache memory 601-607, the cache row address registers 701-707, as shown in FIG. 3 of Lee, can neither disclose, teach nor suggest the eviction buffer recited by Claim 23.

Moreover, if the Examiner relies on memory system 300, as shown in FIG. 3 of Lee, to anticipate the above recited features of Claim 23, Applicant respectfully submits that memory banks 301, 302, 303 and 304 of memory 300 do not each include at least one memory device and

a data cache coupled to an eviction buffer, both coupled to the memory device, as required to disclose the at least two memory modules recited by Claim 23.

Accordingly, for at least the reasons indicated above, Applicant respectfully submits that the Examiner is prohibited from relying on Lee as an anticipatory reference since Lee fails to exactly disclose each and every element recited by Claim 23, and specifically the at least two memory modules each including a memory device and a data cache coupled to an eviction buffer, both coupled to the memory device, as recited by Claim 23. Banner Titanium, supra.

Consequently, Applicant respectfully submits that the Examiner fails to establish a *prima facie* case of anticipation with Lee as an anticipatory reference, since the Examiner fails to illustrate that the single prior art reference disclosure of Lee includes the presence of each and every element recited by Claim 23. Lindemann, supra.

Therefore, for at least the reasons provided above, Claim 23 is patentable over Lee, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claim 23.

II. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 20-22 and 24-25 under 35 U.S.C. §103(a) as being unpatentable over Lee in view of U.S. Patent No. 5,526,510 issued to Akkary et al. ("Akkary"). Applicant respectfully traverses this rejection.

Regarding Claim 20, Claim 20 recites a memory module, which includes the following claim features, which are neither taught nor suggested by the combination of Lee in view of Akkary:

> at least one memory device; and
> a data cache coupled to an eviction buffer, both coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller over a memory bus,
> the memory module to receive a write-back command, the write-back command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device. (Emphasis added.)

As indicated above with regard to the §102(b) rejection of Claim 23, the cache row address registers 701-707 as illustrated with reference to FIG. 3 of Lee, are used to store a cache address corresponding to each cache entry in channel row cache memories 601-607. (See col. 8, lines 41-47.) Accordingly, since cache row address registers 701-707 do not store previous data evicted from the channel row cache memories 601-607, Lee cannot teach that evicted data is stored within cache row address registers 707 nor that such evicted data is written out of the registers 701-707 to the memory banks 301-304, as recited by Claim 20.

Regarding the Examiner's citing of Akkary, assuming arguendo, that Akkary teaches the features performed by the memory module in response to a writeback command, as recited by Claim 20, modifying of Lee to write the cache addresses stored within cache row address registers 701-707 to memory banks 301-304, as recited by Claim 23, results in the addresses stored within address registers 701-707 being written out of registers 701-707 to memory banks 301-304. However, for at least the reasons indicated above, memory banks 301-304, as taught by Lee, are used to store data, and not the addresses corresponding to such data.

As mandated by case law, to establish a *prima facie* case of obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Here, Lee fails to teach or suggest a memory module including at least one memory device, which is coupled to both a data cache and an eviction buffer, as recited by Claim 20. Furthermore, the Examiner's citing of Akkary fails to rectify the deficiencies of Lee in teaching the data cache and eviction buffer coupled to the memory device of the memory module recited by Claim 20.

For at least the reasons indicated above, since the cache row address registers 701-707, as taught by Lee, neither teach nor suggest an eviction buffer, as recited by Claim 20, one skilled in the art would not modify, and could not modify Lee, as taught by Akkary, to write data addresses from registers 701-707 to the memory banks 301-304 (see FIG. 3 and 5 of Lee) since storage of such addresses could result in the loss of data from channel row cache memories 601-607. Accordingly, Applicant respectfully submits that the combined teachings of Lee in view of Akkary would not have suggested the claimed subject matter to one of ordinary skill in the art.

Consequently, Applicant respectfully submits that the prior art combination of Lee in view of Akkary fail to teach or suggest all claim features recited by Claim 20, as required to establish *prima facie* obviousness. Id.

Therefore, Applicant respectfully submits that Claim 20 is patentable over the combination of Lee in view of Akkary. Id. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 20.

Regarding Claims 21 and 22, Claims 21 and 22, based on their dependency from Claim 20, are also patentable over the combination of Lee in view of Akkary. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 21 and 22.

Regarding Claims 24 and 25, Claims 24 and 25, based on their dependency from Claim 23, would also be patentable over the combination of Lee in view of Akkary, since Akkary fails to rectify the deficiencies of Lee in teaching or suggesting the eviction buffer recited by Claim 20. Therefore, for at least the reasons provided above, Applicant respectfully submits that Claims 24 and 25, based on their dependency from Claim 23, are also patentable over the combination of Lee in view of Akkary. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 24 and 25.

The Examiner has rejected Claims 9, 11-12 and 16-19 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,378,049 issued to Stracovsky et al. ("Stracovsky") in view of Lee and Akkary. Applicant respectfully traverses this rejection.

Regarding Claim 9, Claim 9 recites a memory module including the following features, which are neither disclosed, taught nor suggested by the combination of Stracovsky in view of Lee and further in view of Akkary:

> at least one memory device, and
> a data cache coupled to an eviction buffer, both coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into the eviction buffer. (Emphasis added.)

Applicant respectfully submits that the above-recited features of Claim 9 regarding a memory module including at least one memory device coupled to both a data cache and an eviction buffer are analogous to the above-recited features of Claim 20. Accordingly, Applicant's arguments provided above with regard to the §103(a) rejection of Claim 20 apply to the Examiner's §103(a) rejection of Claim 9.

As indicated by the Examiner, Stracovsky does not teach a memory module including at least one memory device and a data cache coupled to an eviction buffer, both coupled to the memory device (see p. 8, ¶ 002 of the Office Action mailed 8/9/06.). As a result, The Examiner cites Lee. As previously indicated, the Examiner has incorrectly interpreted cache row address registers 701-701 (see Lee, FIG. 3) as an eviction buffer, as recited by Claim 9. Hence, for at least the reasons indicated above, Lee also does not teach or suggest the memory module recited by Claim 9.

Consequently, Applicant respectfully submits that the combination of Stracovsky in view of Lee and further in view of Akkary, cannot teach all claim features recited by Claim 9, as required to establish a *prima facie* case of obviousness. Id. Therefore, for at least the reasons provided above, Applicant respectfully submits that Claim 9 is patentable over the prior art combination of Stracovsky in view of Lee and further in view of Akkary.

Hence, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 9, as well as the §103(a) rejection of Claims 11-12, which based on their dependency from Claim 9, are also patentable over the combination of Stracovsky in view of Lee and further in view of Akkary.

Regarding Claim 16, Claim 16 recites the following claim features, which are neither disclosed nor suggested by the combination of Stracovsky in view of Akkary:

> an array of tag address storage locations; and
> a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache and an eviction buffer located on at least one memory module of a system memory, the command sequencer and serializer to deliver a writeback command to the eviction buffer associated with the memory module, the writeback command to cause a previous line of data evicted from the data cache

and stored in the eviction buffer, to be written out to a memory device of the memory module. (Emphasis added.)

Applicant respectfully submits that the above-recited features of Claim 16 regarding a memory module including at least one memory device coupled to both a data cache and an eviction buffer are analogous to the above-recited features of Claim 9. Accordingly, Applicant's arguments provided above with regard to the §103(a) rejection of Claim 9 apply to the Examiner's §103(a) rejection of Claim 16.

As recited by Claim 16, issuance of the writeback command to the eviction buffer associated with the memory module causes a previous line of data, evicted from the data cache and stored in the eviction buffer, to be written out to a memory device of the memory module. As correctly noted by the Examiner, Stracovsky fails to teach or suggest a data cache and an eviction buffer located on at least one memory module of the system memory. (See, p. 10, ¶ 3 of the Office Action mailed 8/9/06.) As a result, the Examiner cites Lee. As previously indicated, the Examiner has incorrectly interpreted cache row address registers 701-701 (see Lee, FIG. 3) as an eviction buffer, as recited by Claim 16. Hence, for at least the reasons indicated above, Lee also does not teach or suggest the memory module recited by Claim 16.

Consequently, Applicant respectfully submits that the prior art combination of Stracovsky in view of Lee and further in view of Akkary, fails to at least teach or suggest a data cache and an eviction buffer located on at least one memory module of the system memory, as recited by Claim 16.

Therefore, Applicant respectfully submits that the Examiner fails to establish a *prima facie* case of obviousness of Claim 16, with the prior art combination of Stracovsky in view of Lee and further in view of Akkary, since such prior art combination fails to teach or suggest all claim limitations recited by Claim 16. Id.

Hence, Applicant respectfully submits that Claim 16 is patentable over the combination of Stracovsky in view of Akkary. Id. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 16.

Regarding Claims 17-19, Claims 17-19, based on their dependency from Claim 16, are also patentable over the prior art combination of Stracovsky in view of Akkary. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 17-19.

CONCLUSION

In view of the foregoing, it is submitted that Claims 9, 11, 12 and 16-25 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Annie McNally 10/18/2006
Annie McNally Date